Abstract

A system with multiple processors sharing a single memory module without noticeable performance degradation is described. The memory module is divided into n independently addressable banks, where n is at least 2 and mapped such that sequential addresses are rotated between the banks. Such a mapping causes sequential data bytes to be stored in alternate banks. Each bank may be further divided into a plurality of blocks. By staggering or synchronizing the processors to execute the computer program such that each processor access a different block during the same cycle, the processors can access the memory simultaneously. Additionally, a cache is provided to enable a processor to fetch from memory a plurality of data words from different memory banks to reduce memory latency caused by memory contention.

(Fig. 2)